Scheme – G

Sample Test Paper - I

Course Name : Computer Engineering Group

Course Code : CO/CM/CD/IF/CW

Semester : Third **17333**

Subject Title : Digital Techniques

Marks : 25 **Hours: 1 Hrs.**

Q.1) Attempt any THREE: **09 Marks**

a) Define
   i) Propagation delay
   ii) Fan-in
   iii) Fan-out

b) Convert the following:
   i) $(42)_{10} = (?)_2$
   ii) $(67)_8 = (?)_2$
   iii) $(1101011)_2 = (?)_H$

c) Draw the symbol, logical Expression & truth table of the following gates.
   i) AND gate
   ii) Ex – OR gate

d) Design anHalf Adder circuit with truth table, K – map and logical circuit diagram.

Q. 2) Attempt any TWO: **08 Marks**

a) Compare TTL & CMOS logic families on the basis of

   i) Propagation delay ii) Fan-in iii) Fan-out iv) Power dissipation.

b) State and prove De Morgan's theorem.

c) Reduce the following Boolean expression using K – map.

   $Y = \Sigma\, m_0, m_2, m_4, m_6, m_8, m_9, m_{10}, m_{12}, m_{13}, m_{14})$

   Draw the logical circuit diagram of the simplified expression using basic gates

Q.3) Attempt any TWO: **08 Marks**

a) Subtract using 1's Complement & 2's complement method.

   $(110100)_2 - (111000)_2$

b) Draw the logical circuit diagram of AND, OR, NOT & NOR gates using NAND gates.

c) Simplify the following Boolean expressions.
   i) $Y = A\overline{B} + \overline{A.B} + B\overline{C}$
   ii) $Y = AB + B(\overline{B}+C) + A\overline{B}$

Scheme – G

Sample Test Paper - II

Course Name : Computer Engineering Group

Course Code : CO/CM/CD/IF/CW

Semester : Third **17333**

Subject Title : Digital Techniques

Marks : 25 **Hours: 1 Hrs.**

Q.1) Attempt any THREE: (3x3) **09 Marks**

a) State the need for multiplexers. Draw the block diagram of 4:1 Mux.

b) Differentiate between combinational logic & Sequential logic circuits (any 3 points).

c) Draw a clock signal and explain positive edge triggering & negative edge triggering.

d) Define the following specifications of A – D convertor

i) Quantization noise ii) Conversion Time iii) Resolution

Q.2) Attempt any TWO: (2x4) **08 Marks**

a) Draw the block diagram of BCD to 7 – segment decoder/ driver and draw its truth table. Give the function of Lamp Test and Ripple Blanking input pins.

b) What is Race- around condition in JK flip flop and how it can be eliminated?

c) Draw the logical circuit diagram of 3 – bit ripple counter and draw its timing diagram showing clock and outputs of each flip Hop.

Q.3) Attempt any TWO: (2x4) **08 Marks**

a) Draw the circuit diagram of weighted resistors method of D-A converter and describe its working.

b) Draw the logical circuit of serial-in serial-out shift register. Explain with Truth table.

c) i) Describe the significance of Preset& Clear terminal in J-K flip flop

iii) Convert S-R flip flop into D- flip flop and explain the working.

Scheme – G

Sample Question Paper

Course Name : Computer Engineering Group

Course Code : CO/CM/CD/IF/CW

Semester : Third

Subject Title : Digital Techniques **17333**

Marks : 100 **Hours: 3 Hrs.**

Q.1) (A) Attempt any SIX. **12 Marks**

a) Define with respect to digital ICs
   i) Propagation delay
   ii) Noise immunity
b) What is positive logic with respect to a digital signal?
c) Draw the logical symbol, Truth table, and logical expression of AND gate.
d) State any four Boolean Laws.
e) Solve the following:
   i) $(110101)_2 + (101101)_2$
   ii) $(1010)_2 - (1000)_2$ using 1's complement method.
f) Draw the symbol, logical expression and truth table of 3i/p OR gate.
g) Draw the truth table of digital comparator IC 7485.
h) Define the following with respect to DAC
   i) Resolution
   ii) Settling time.

Q.1) (B) Attempt any TWO. **08 Marks**

a) Convert the following
   i) $(212)_{10} = (?)_2$
   ii) $(11010)_2 = (?)_{10}$
   iii) $(436)_8 = (?)_2$
   iv) $(206)_8 = (?)_H$
b) State and prove De Morgan's theorem.
c) Perform the following BCD arithmetic.
   i) $(247)_{10} + (463)_{10}$
   ii) $(42)_{10} - (27)_{10}$

Q.2) Attempt any FOUR: **16 Marks**

a) Implement AND & OR gates using NAND gates only.

b) Given $Y = A\overline{B} + \overline{BC} + \overline{A}C$

   Implement the logical expression using gates.

c) Perform the following binary operation
   i) 11010×1011
   ii) $11011 \div 110$
d) Design a Half Adder Circuit.
e) Minimize the following Boolean expression using K – map.

$Y = \Sigma\, m_1, m_3, m_5, m_7, m_{10}, m_{11}, m_{14}, m_{15}$. Draw the logical circuit diagram of minimized expression using basic gates

f) Draw the block diagram of Decimal to BCD encoder IC 74147 and describe its working with truth table.

Q.3) Attempt any FOUR: 16 Marks

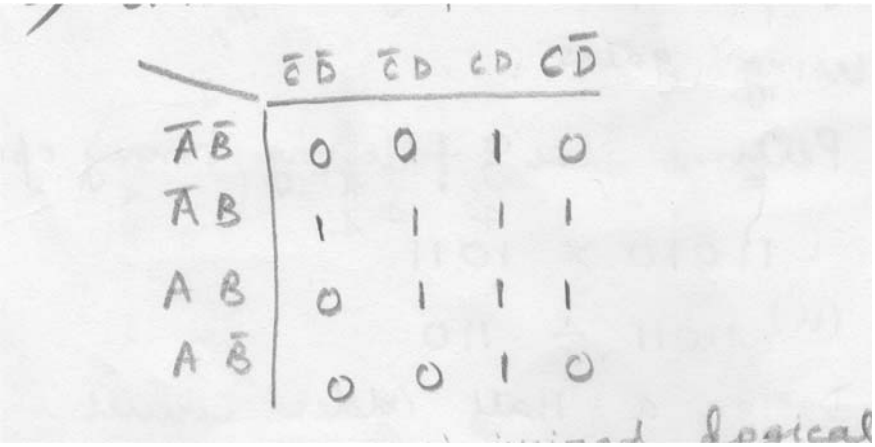
a) Simplify the following Boolean Expression using Boolean laws.

i) $Y = \overline{A}B + ABD + A\overline{B}C\overline{D} + BC$

ii) $Y = \overline{A} + \overline{AB} + \overline{A}\ B\ \overline{C} + \overline{A}\ \overline{B}\ C\ D$

b) Draw the logical block diagram of 4:1 multiplexers and describe its working. Give the expression for the output and draw the circuit diagram using gates.

c) Given K-map



Write the minimized logical expression and draw the logical circuit using universal gates.

d) Standardize the following Boolean expression

i) $Y = AB + \overline{B}C + A\overline{C}$

ii) $Y = (A+C).\ (B+\overline{C}) + (\overline{A}+B)$

e) Draw the logical circuit diagram of clocked SR flip flop using NAND gates and describe its working with truth table.

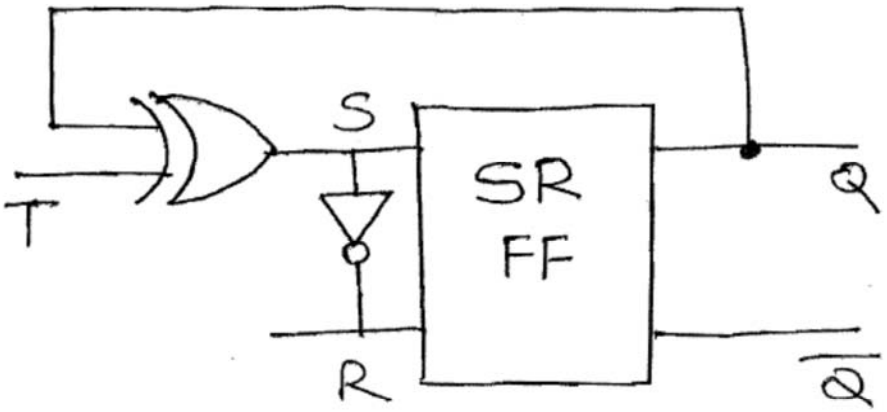
f) Draw the logical circuit diagram of a 3 bit asynchronous UP Counter. Describe its working with timing diagram.

Q.4) Attempt any FOUR: 16 Marks

a) What is modulus of a counter? Show the method to determine the number of flip flops for a mod – 46 Counter?

b) Give 2 advantages and 2 disadvantages of A – D Converters.

c) Prepare the truth table for the given logical Circuit diagram and from the truth table identify the flip flop.



d) Explain the significance of Preset & Clear terminals with truth table of JK Flip flop.
e) Classify memories. What are the mechanisms used for erasing EPROM.
f) Draw the block diagram of successive approximation method of A-D Converter & describe its working.

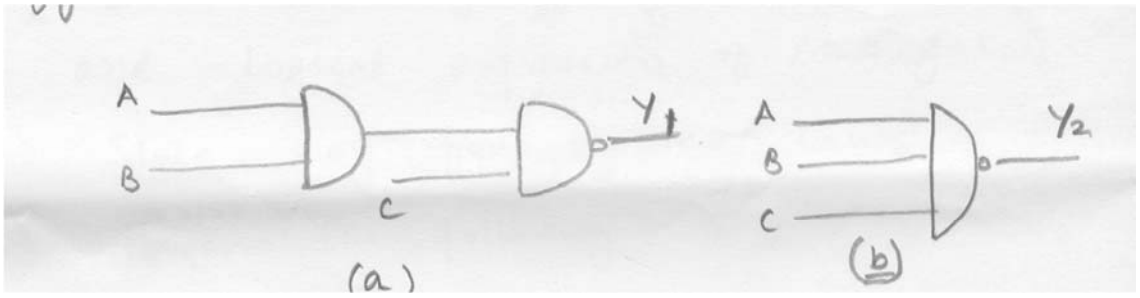
Q.5) Attempt any FOUR: 16 Marks

a) Perform the following Subtraction using 2's complement method.
   i) 1000 – 01001
   ii) 11100 – 00011
b) Draw the block diagram of Sequential logic and state the importance of clock signal in it.
c) Given logical equation
   $Y = (A+BC)(B+\bar{C}\bar{A})$
   Design a circuit using basic gates to realize this function.
d) Draw the circuit of a ring counter and describe with timing diagram.
e) Draw the block diagram of BCD – 7 segment decoder / driver. Describe its working.
f) Draw the logical circuit diagram of PISO shift register. Describe its working.

Q.6) Attempt any TWO: 16 Marks

a) i) State the applications of de multiplexers. (2 Marks)
   ii) Design 16:1 multiplexer using 4:1 multiplexers only. (6 Marks)

b) i) Determine the output of the following figures and shows that $Y_1 = Y_2$.(2 marks)



   ii) State two applications of shift registers. (2 marks)
   iii) Draw a mod 5 asynchronous counter. Explain in brief. (4 marks)

c) i) Draw the Circuit diagram of R – 2R Ladder method of D – A Converter and describe its working. (4 Marks)
   ii) A D/A converter has a full scale analog o/p of 10 V and accepts 4 binary bits as inputs. Find the Voltage Corresponding to each analog step. (4 marks)